Voltage Optimization for State of the Art RF-LDMOS for 2.1GHz W-CDMA Cellular Infrastructure Applications

Helmut Brech, Wayne Burger, Chris Dragon, and Bob Pryor

RF & DSP Infrastructure Division, Semiconductor Products Sector, Motorola, 2100 East Elliot, Tempe, AZ 85284, e-mail: Helmut.Brech@motorola.com

Abstract — **The breakdown and operating voltage optimization of a RF-LDMOS power amplifier (PA) transistor for high power base station applications is presented. For a given device a local maximum in linear PAE is observed to be a function of the drain supply voltage. Best results were achieved for an optimized 10mm device with a supply voltage of 32V. W-CDMA results (single carrier W-CDMA 3GPP signal at 2.14GHz, 8.5dB P/A) were 29% PAE with Pout=162mW/mm at –45dBc ACP, and 62% PAE with Pout=785mW/mm at P3dB with tuning for optimum back-off performance. To our knowledge these results represent the highest PAE's for this back-off level ever reported for transistors of any material that are appropriate for high power infrastructure applications, as well as state of the art peak power densities for silicon [1].**

I. INTRODUCTION

With the delayed rollout of 3rd generation cellular networks future generation networks operating at much higher frequencies seem to be pushed out for years. This keeps much of the attention in the cellular infrastructure market on systems operating at 2.1 GHz and below. Silicon LDMOS power transistors have been proven to be not only reliable and cost effective but also superior for high power linear applications compared to other transistor technologies. One of the most important performance parameters is the efficiency at some linearity criteria. Good power and voltage scalability of a technology are key to realize most of the intrinsic device capability in high power applications. This flexibility allows to design devices for various system level requirements like for envelope tracking which requires good performance at a certain supply voltage as well as the capability to handle significantly increased voltages for a certain period of time [2,3]. In this paper we report the breakdown voltage optimization of devices operating under various supply voltages.

II. DEVICES EXPERIMENTS

LDMOS devices with different BVdss in the range of 68V to 91V were fabricated on a single wafer. To obtain various breakdown voltages only the length of their

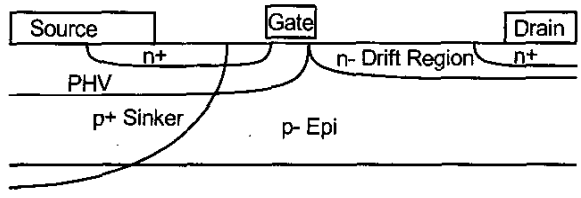

Fig. 1. Schematic cross section of a LDMOS transistor.

n- drift region was varied as shown in the schematic LDMOS cross section of Fig. 1. Changing only this length minimizes second order effects and other ambiguity. However, additional device fabrication features would have to be taken into account for a final optimization. The breakdown voltages and the corresponding Rdson values are shown in Fig. 2. The linear Rdson increase is as expected since only the drift region is increased and all other parameters are kept constant. The fact that BVdss is increased almost linearly with increasing the drift region extension suggests that the breakdown is not vertically limited (that is not limited by junction depths and epi thickness) which was intended to allow this kind of experiment. Breakdown voltages of well over 100V can be obtained with fairly minor additional changes.

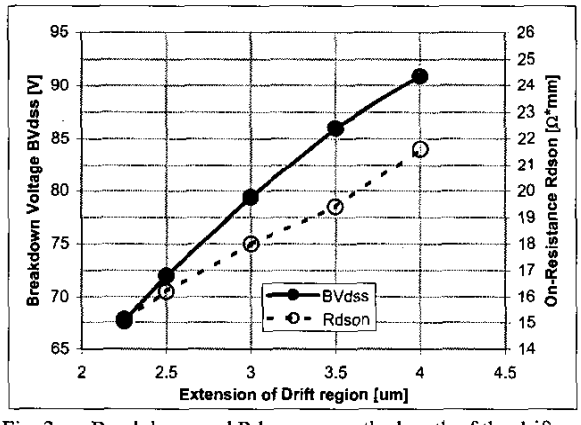

Fig. 2. Breakdown and Rdson versus the length of the drift region of otherwise identical devices.

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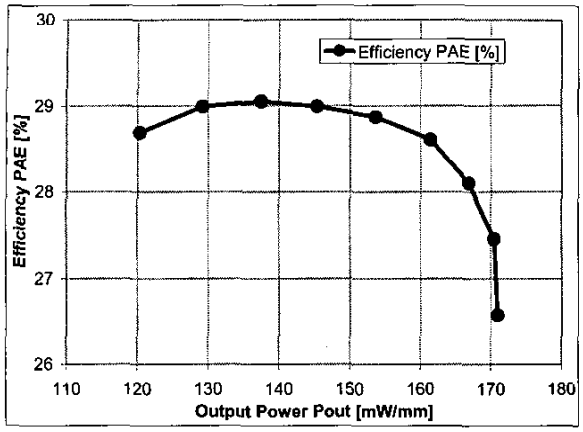

Fig. 3. Typical trade-off between PAE and Pout @-45dBc ACP for different load impedances with a constant magnitude and varied angle.

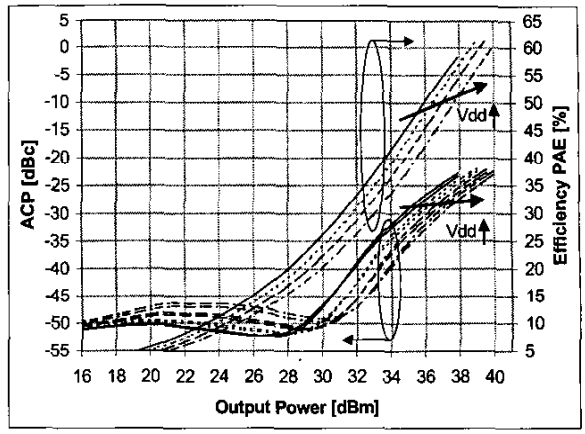

Fig. 4. Upper and lower adjacent channel power (ACP) and power added efficiency of one sample transistor versus output power for drain supply voltages of 28V, 32V, 36V, and 40V.

III. Single Carrier W-CDMA Load Pull

The RF characterizations were done using transistors with 10mm gate periphery in a ceramic package mounted in a fixture on a copper block with no active cooling. The 10mm periphery was chosen to put the source and load into a good tuning range with only a 2:1 fixture impedance transformation while already providing some meaningful power levels. The optimizations were performed by individually tuning the devices for various supply voltages on a load pull system using a single carrier W-CDMA 3GPP signal at 2.14GHz. Since W-CDMA applications demand very high linearity we set the main criteria to be the maximum power added efficiency (PAE) in back-off at -45dBc ACP and a maximum input return loss of –10dB. The main remaining decision is a trade-off between the output power and the efficiency for different load tuning points. The trade-off range is depicted as an example in Fig. 3 where Pout and PAE at –45dBc ACP are shown for different complex loads. The loads used in Fig. 3 were along a line in the Smith chart with a constant magnitude and varying angle. For this particular case the "optimum" was chosen at 28.9% PAE and 155mW/mm, a slightly degraded PAE from its peak of over 29% in order to obtain a substantial output power increase.

IV. Load Pull Results

Fig. 4 plots the PAE and the upper and lower ACP for one sample transistor for drain supply voltages of 28V, 32V, 36V, and 40V. In all cases the upper and lower ACP characteristics are very balanced typically resulting in less than 1.5dBc of ΔACP throughout the entire power drive-up. For the lowest supply voltage of 28V both upper and lower ACP are better than –50dBc up to 29dBm of output power and about 23% efficiency. As expected, the output power increases for a constant ACP and the efficiency decreases for a constant power with increasing supply voltage. To compare device performance, PAE was determined for each sample transistor for all measured supply voltages at the linearity criteria of -45dBc ACP. Since the source and drain impedance optimization of the devices was performed in back-off the typical expectations for voltage, efficiency and output power trade-off no longer hold true. For varying the supply voltage we found a local maximum in efficiency for each device as shown in Fig. 5. The lower the breakdown voltage the lower the drain voltage at which

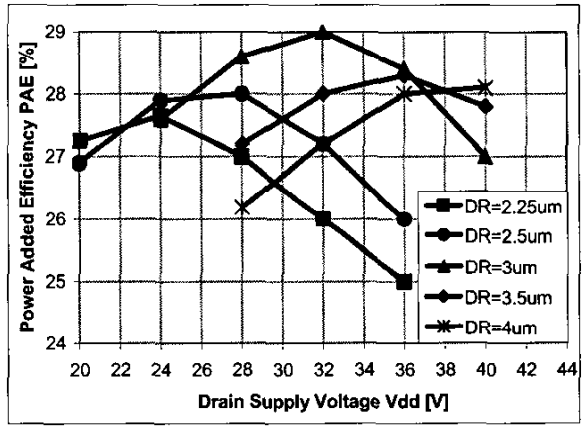

Fig. 5. PAE @-45dBc ACP versus drain supply voltage for devices with different drift region (DR) extensions, i.e. different breakdown voltages.

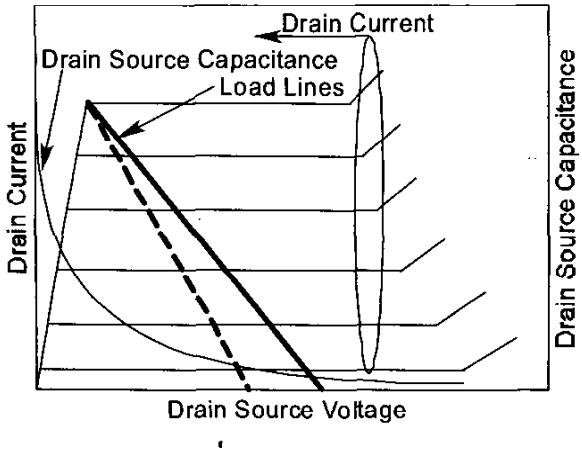

Fig. 6. Schematic IdVd characteristics of a transistor along with a typical output capacitance. Load lines are over laid to demonstrate operation at different supply voltages.

the peak PAE occurs.

The main reasons for reduced efficiency for lower and higher supply voltages are the following: If the device is operated at relatively low voltages the load line for maximum efficiency can be steeper with respect to the device's IdVd characteristics. This is assuming a fixed maximum drain current and fixed knee voltage as shown schematically in Fig. 6. If the device was ideal this would lead to an increased efficiency because for a constant power the device is operated closer to saturation. This can be also seen in the measurements of Fig. 4. If however linearity constraints are taken into account the picture changes since the feedback and output capacitances of the device increase significantly for lower drain voltages as shown by the drain source capacitance in Fig. 6. This means that for a given power the load line swings through an area of higher capacitance that has a negative impact on the efficiency. Moreover, this higher capacitance exhibits a higher slope with respect to the drain voltage, therefore the ideal impedance match is limited to an ever smaller drain voltage swing and thus degrades the linearity. Since the efficiency in Fig. 5 is taken at a given linearity criteria the device has to be backed off a little more to reach the linearity goal therefore reducing the efficiency at that point. After reaching a peak PAE for a given supply voltage it degrades again for very high voltages. This can be attributed to a flatter load line.

The fact that there is a peak PAE for the device with a drift region extension of 3um is attributed to the wafer fabrication process being optimized for that particular layout. It can be assumed that if the devices are individually optimized for their respective breakdown voltage the peak PAE would be very similar for all the devices investigated. This suggests the capability of optimized devices operating in a very wide supply voltage range with similar performance in the back-off regime.

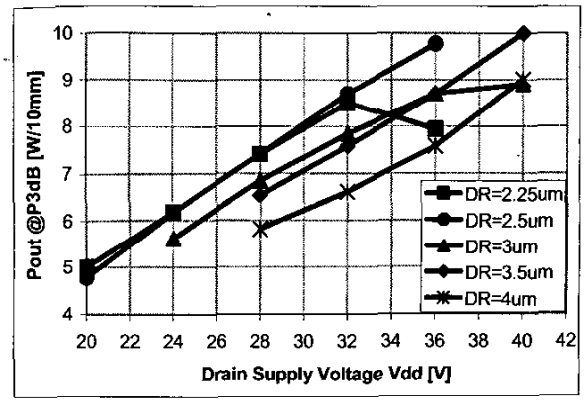

Fig. 7. Output power @-3dB saturated gain (P3dB) versus drain voltage for devices with different drift region extension.

Fig. 7 plots the output power at the 3dB compression point as a function of the drain supply voltage Vdd. The output power increases basically linearly with the drain voltage up to a certain point where it saturates. This is the regime where the RF voltage swing starts to be compressed by the breakdown voltage. The output power is reduced for a given drain voltage for increased drift regions due to the increased Rdson. Since the fixture design limited the supply voltage to about 40V the peak P3dB could not be determined for all devices. However, based on the characteristics in Fig. 7 P3dB well in excess of 10W for the 10mm device would be expected even with the performance optimized for the –45dBc back-off operation.

Fig. 8 shows ACP versus PAE at Vdd=32V for the device with 3um extension. Although the device was optimized at –45dBc it shows exceptional performance at higher power levels including PAE exceeding 60% in saturation.

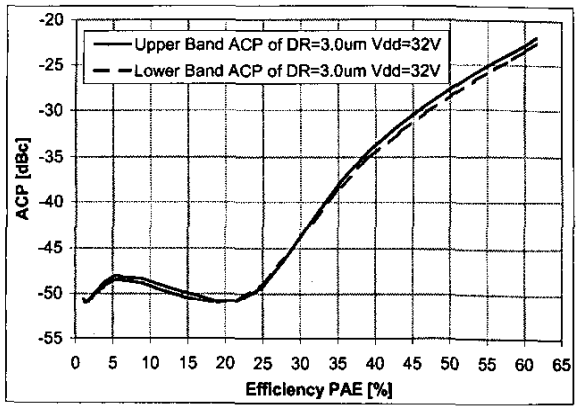

Fig. 8. Upper and lower ACP versus PAE for the device with the highest efficiency.

V. Conclusions

Individual optimization of source and load impedances for an experimental group of LDMOS transistors with various breakdown voltages (BVdss) at various supply voltages has been presented. This optimization has focused on best performance at -45dBc ACP using a single carrier W-CDMA signal at 2.14GHz. In turn, this leads to an optimum choice of supply voltage for a device with a given breakdown voltage. The investigated devices differed only in their drift region length to obtain various breakdown voltages. State of the art back-off device performance for linear applications was demonstrated. While each device reached a local maximum versus supply voltage, the devices showed very high PAE's of over 27.5% @-45dBc ACP over a supply voltage range from 24V to 40V. Peak efficiency of about 29% at –45dBc ACP was obtained and to our knowledge this is the highest reported PAE at this ACP reported of transistors in any material system that are appropriate for high power infrastructure applications. This demonstrates not only exceptional peak performance but also very good scalability in voltage to meet new system requirements.

Acknowledgement

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